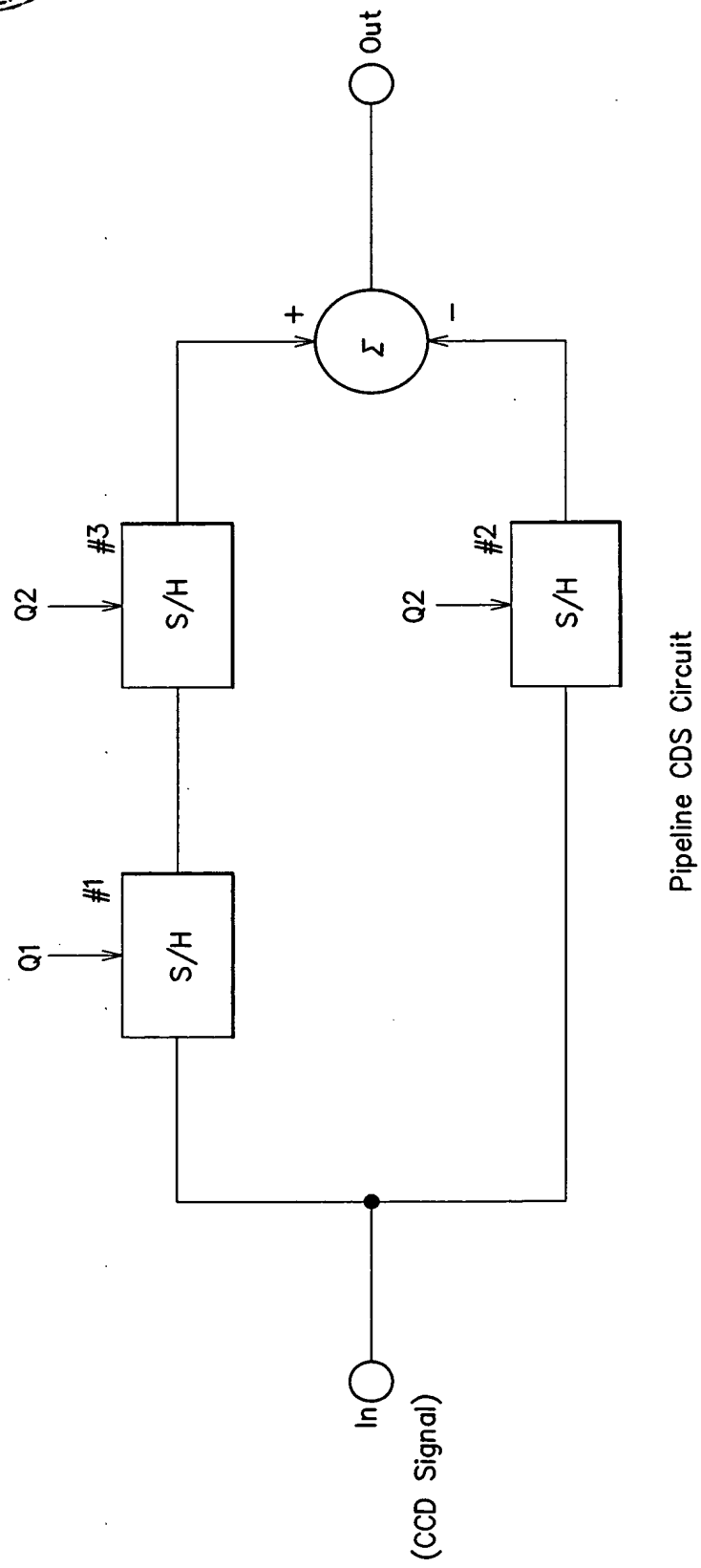

FIG. 1
(Prior Art)

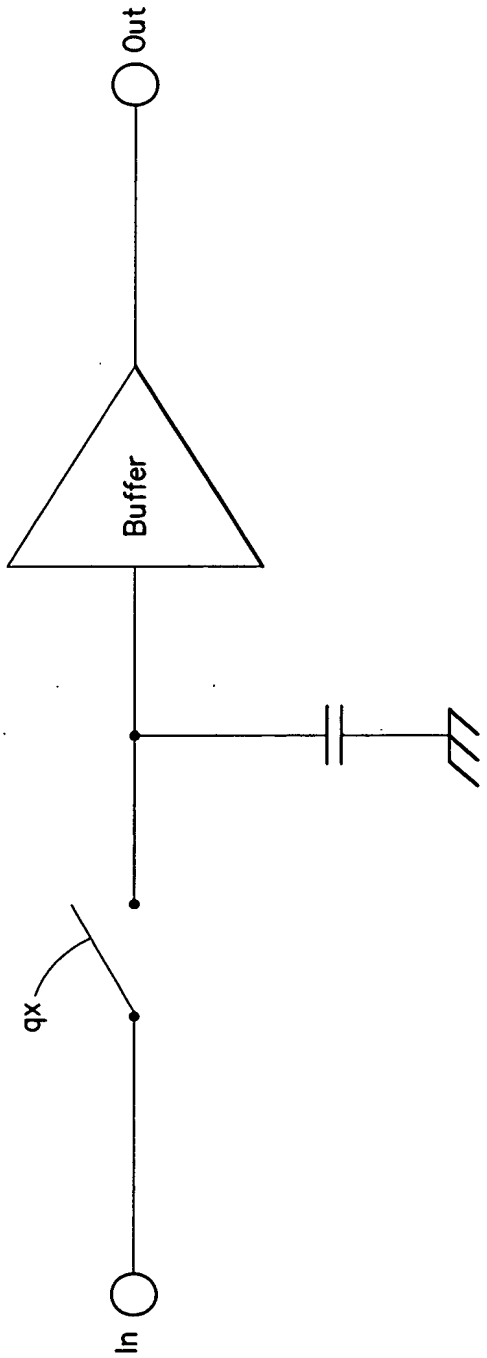

FIG. 2
(Prior Art)

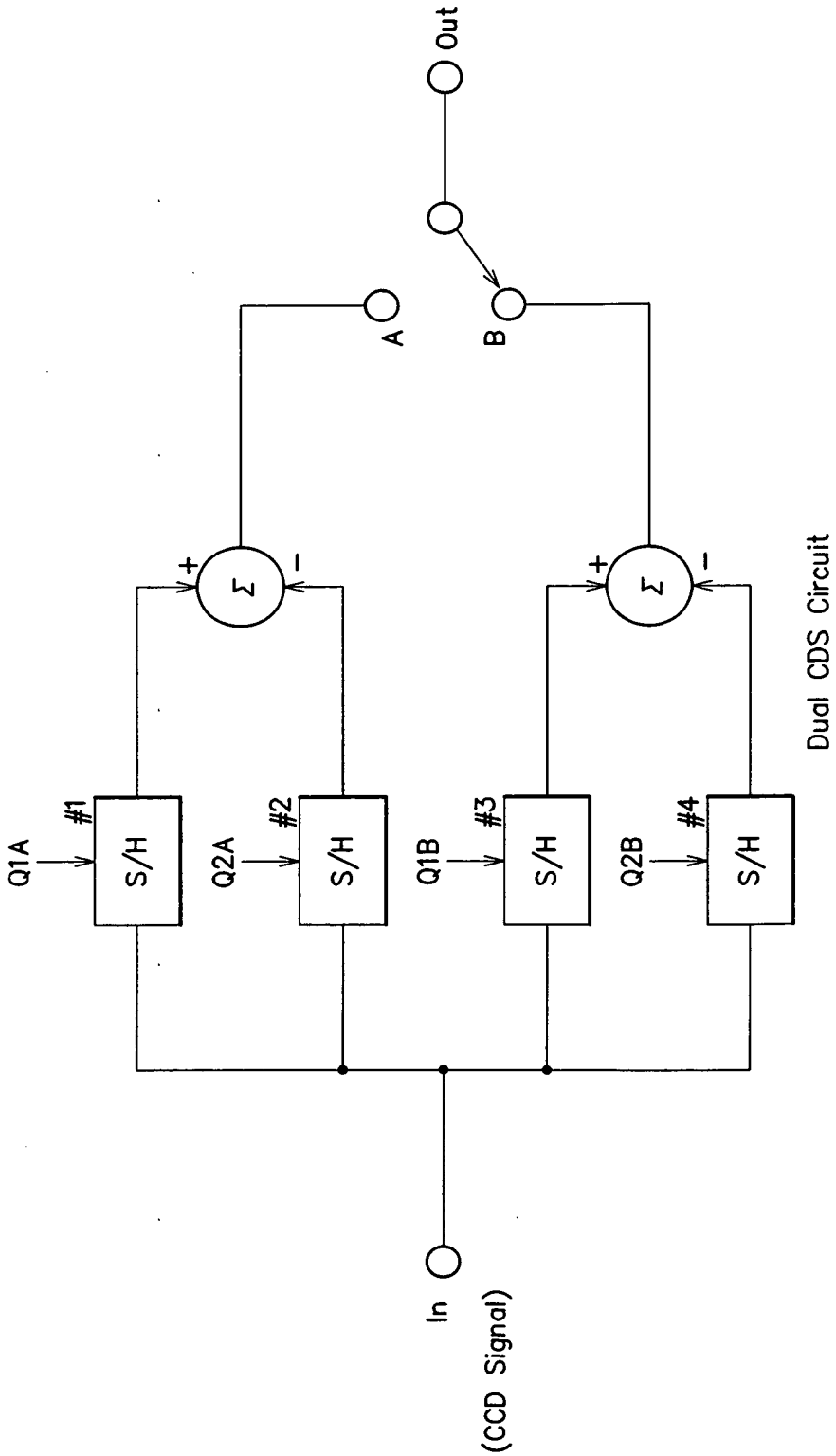

FIG. 3
(Prior Art)

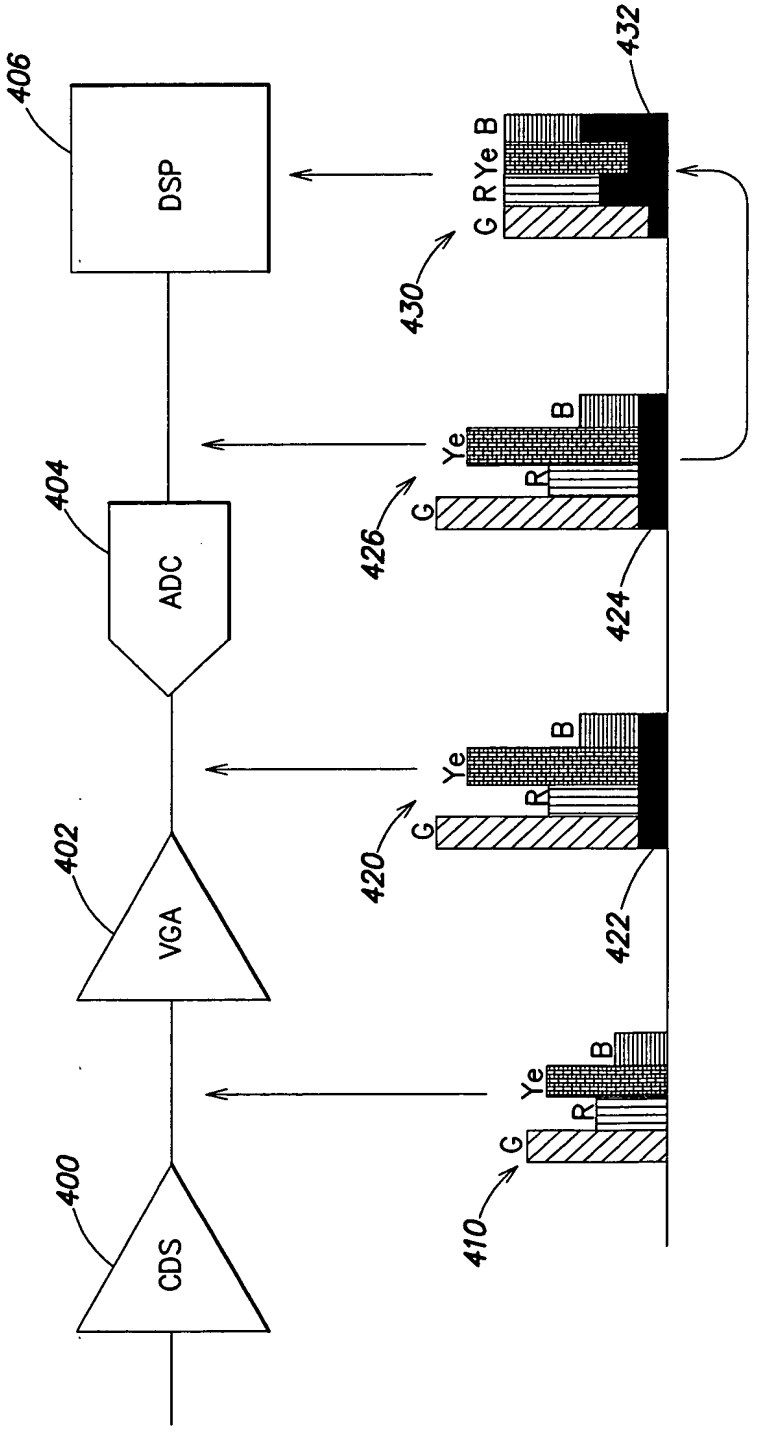

FIG. 4
(Prior Art)

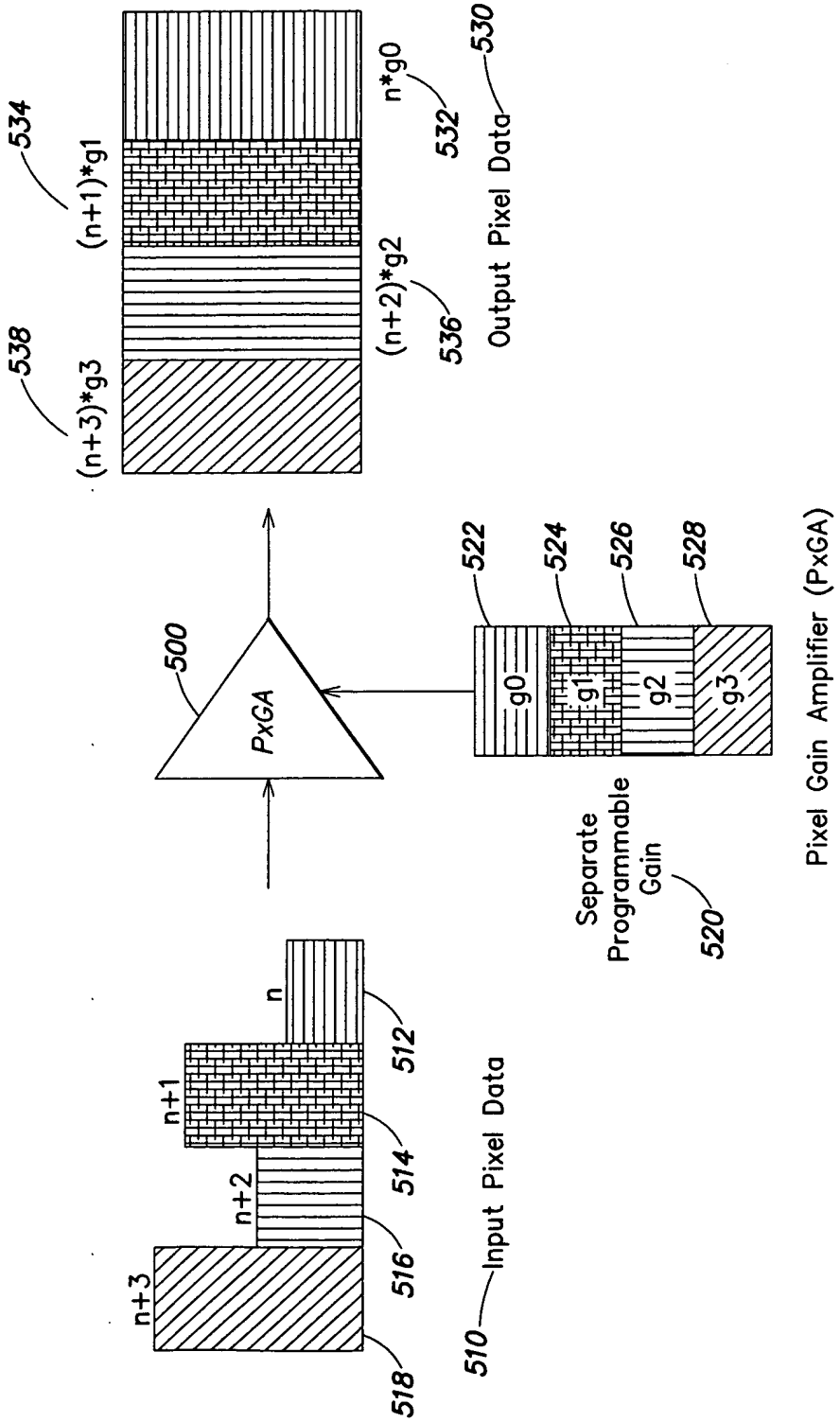
534
(n+1)*g1
n*g0
532
530
Output Pixel Data
538
(n+3)*g3
(n+2)*g2
536
500
PxGA
522
524
526
528
g0
g1
g2
g3
Separate Programmable Gain
520
Pixel Gain Amplifier (PxGA)
n
n+1
n+2
n+3
512
514
516
518
510
Input Pixel Data

FIG. 5

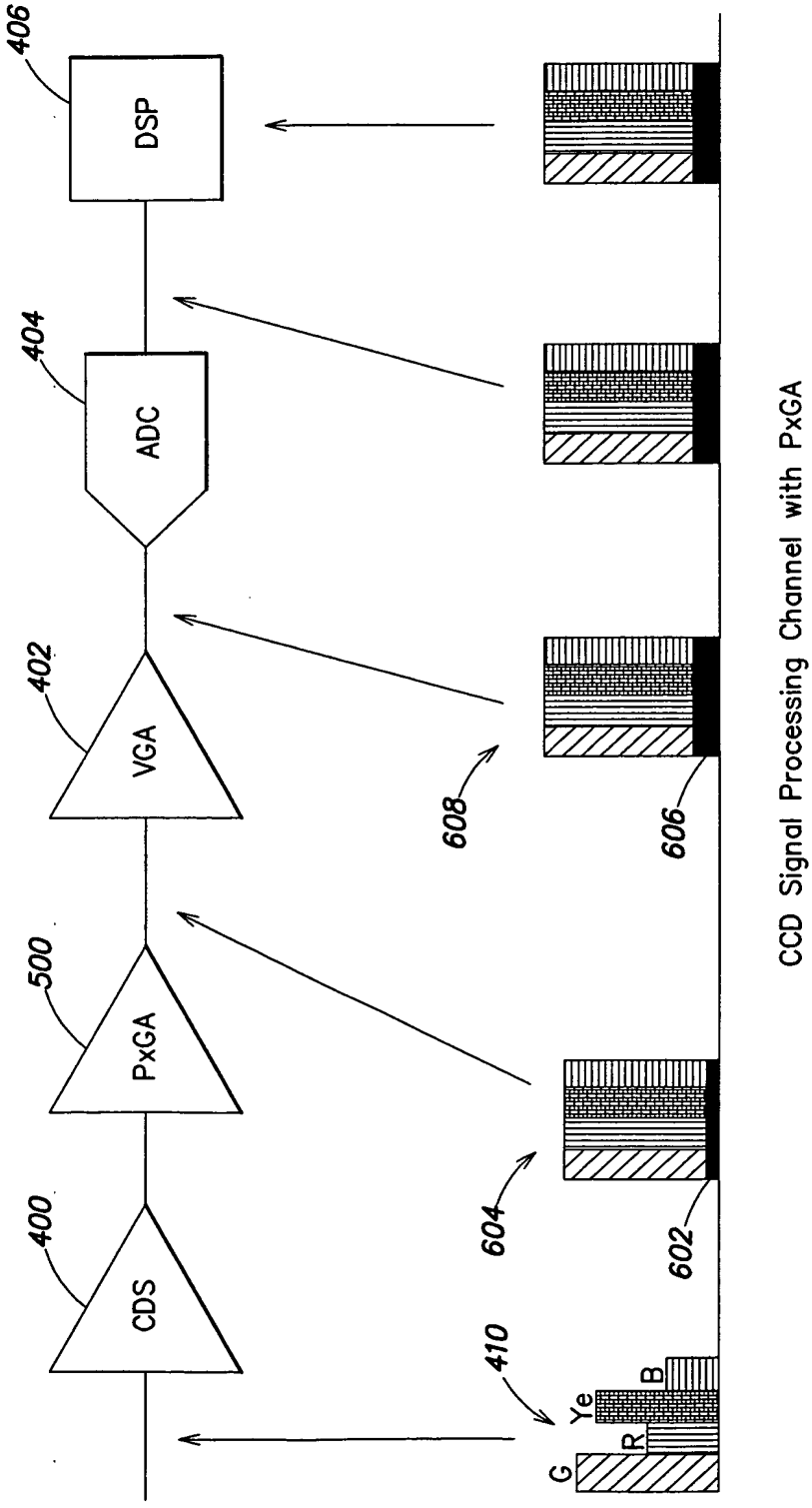
406
DSP
404
ADC
402
VGA
500
PxGA
400
CDS
608
606
604
602
410
B
Ye
R
G
CCD Signal Processing Channel with PxGA

FIG. 6

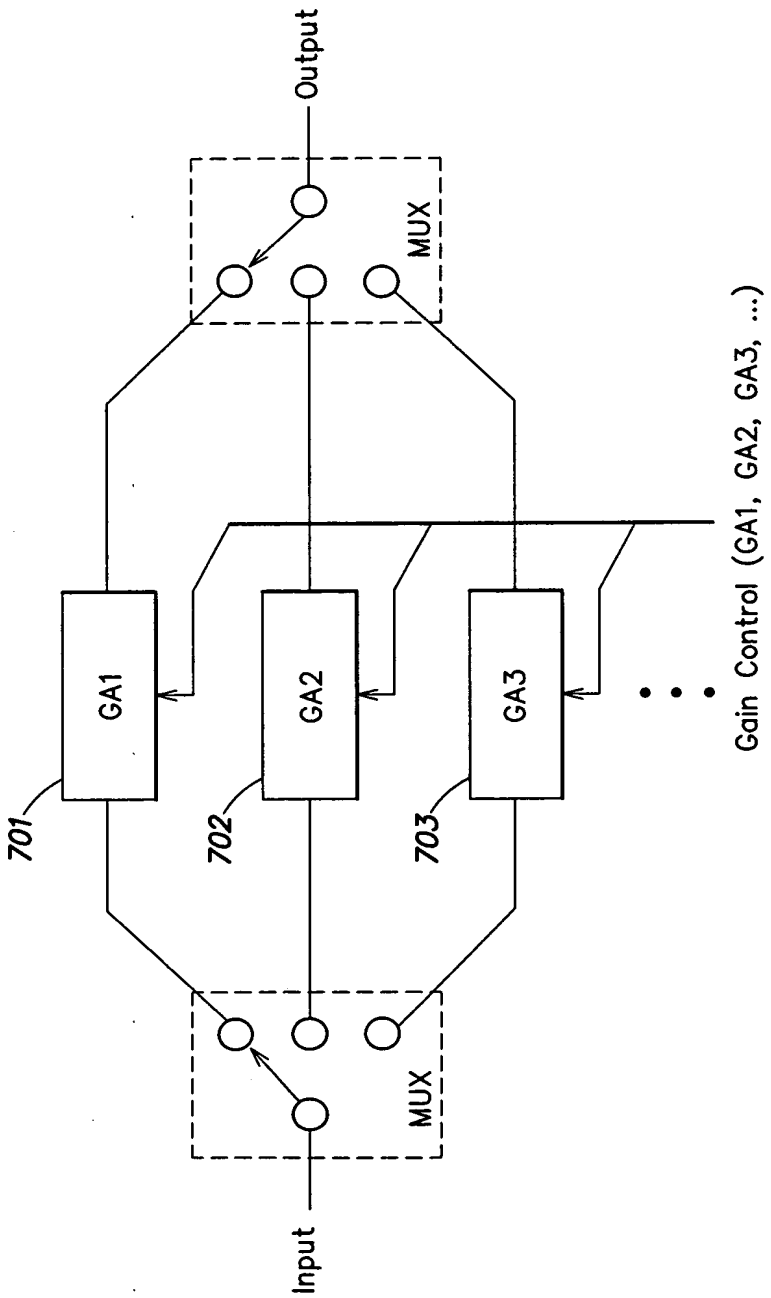

FIG. 7
(Prior Art)

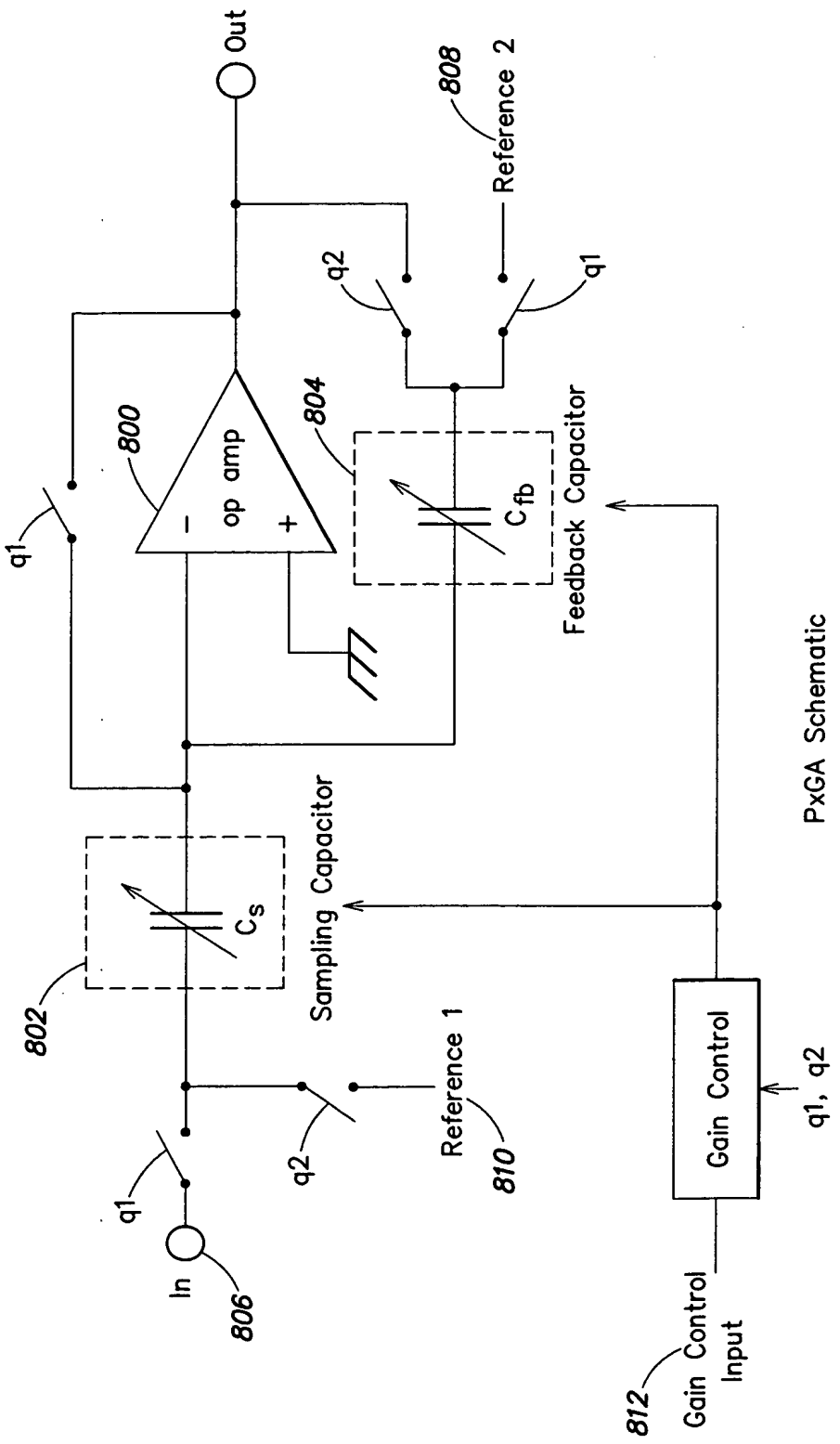
Out
808
Reference 2
q2
q1
800
op amp
804
C_{fb}
Feedback Capacitor
q1
C_s
802
Sampling Capacitor
PxGA Schematic
Reference 1
810
q2
q1
In
806
Gain Control
q1, q2
812
Gain Control Input

FIG. 8(a)

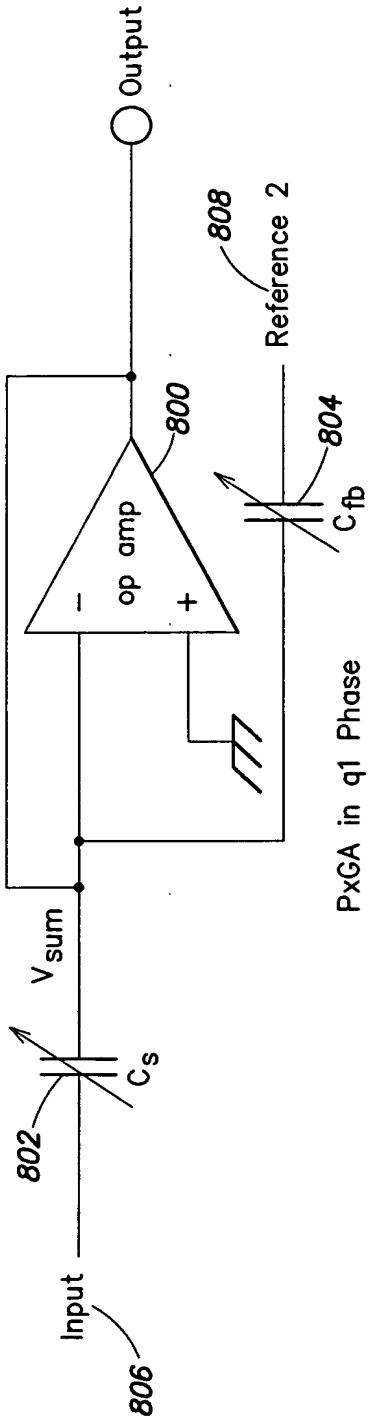
Output
808
Reference 2
800
804
op amp
C_{fb}
V_{sum}
802
C_s
Input
806
PxGA in q1 Phase

FIG. 8(b)

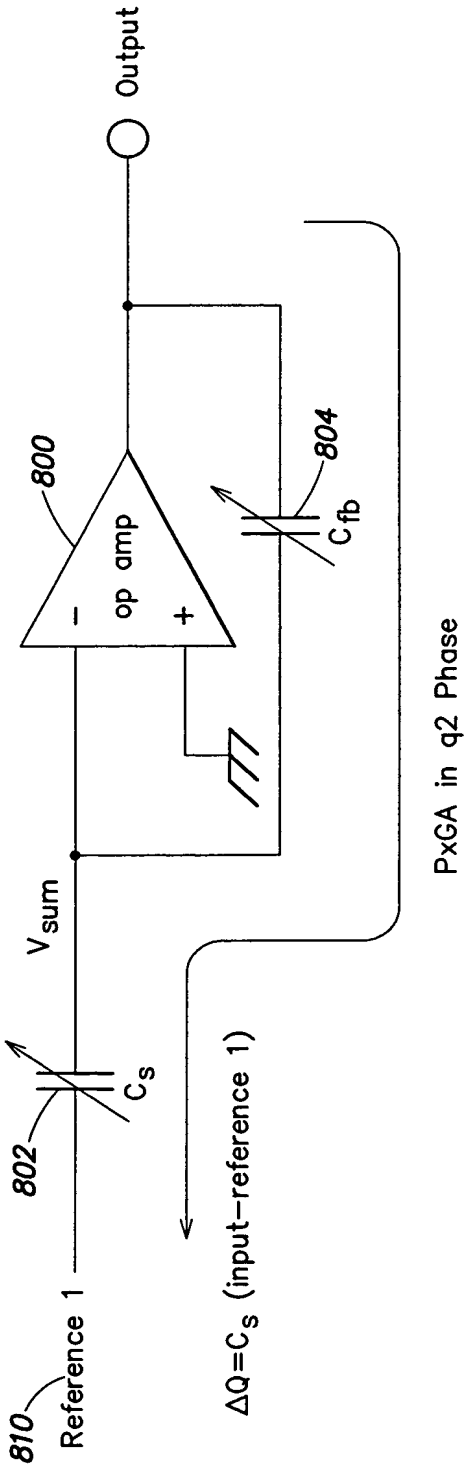
Output
800
804
op amp
C_{fb}
V_{sum}
802
C_s
810
Reference 1
$\Delta Q=C_s$ (input−reference 1)
PxGA in q2 Phase

FIG. 8(c)

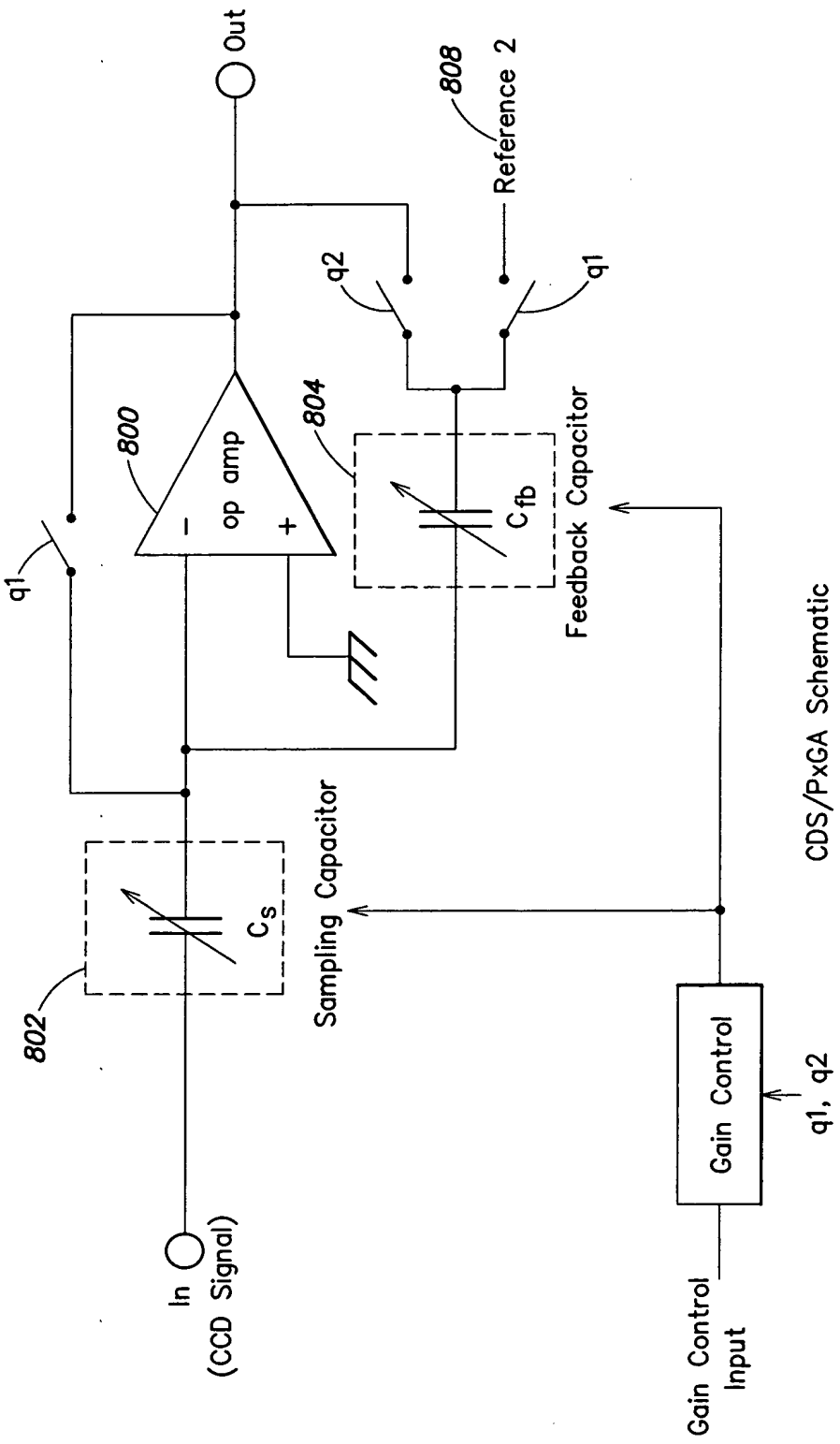
Out
808
Reference 2
q2
q1
800
op amp
804
C_{fb}
Feedback Capacitor
q1
802
C_S
Sampling Capacitor
CDS/PxGA Schematic
In
(CCD Signal)
Gain Control
q1, q2
Gain Control
Input

FIG. 9

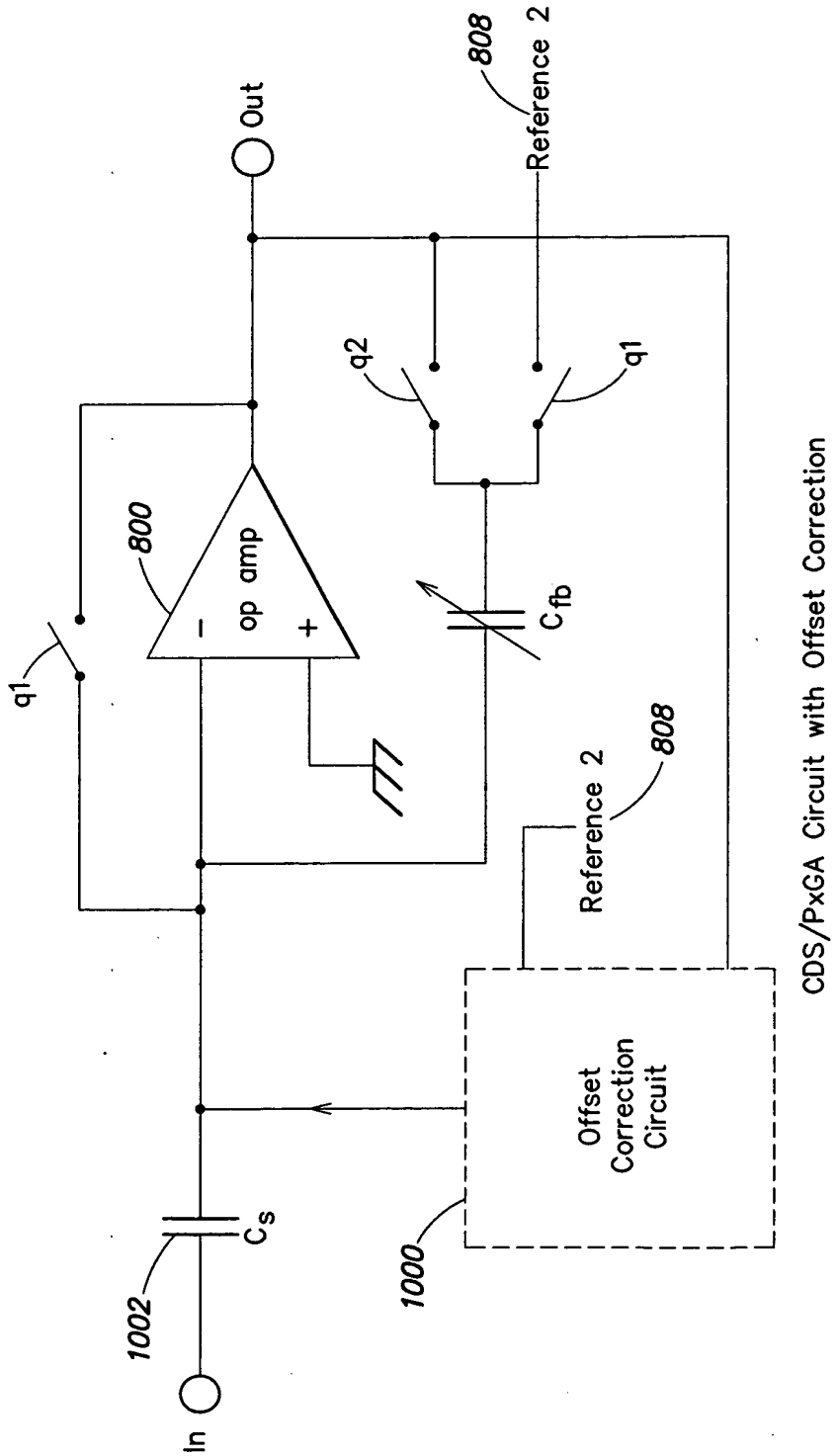
Out
808
Reference 2
q2
q1
800
op amp
-
+
C_{fb}
q1
808
Reference 2
CDS/PxGA Circuit with Offset Correction
Offset Correction Circuit
1000
C_s
1002
In

FIG. 10

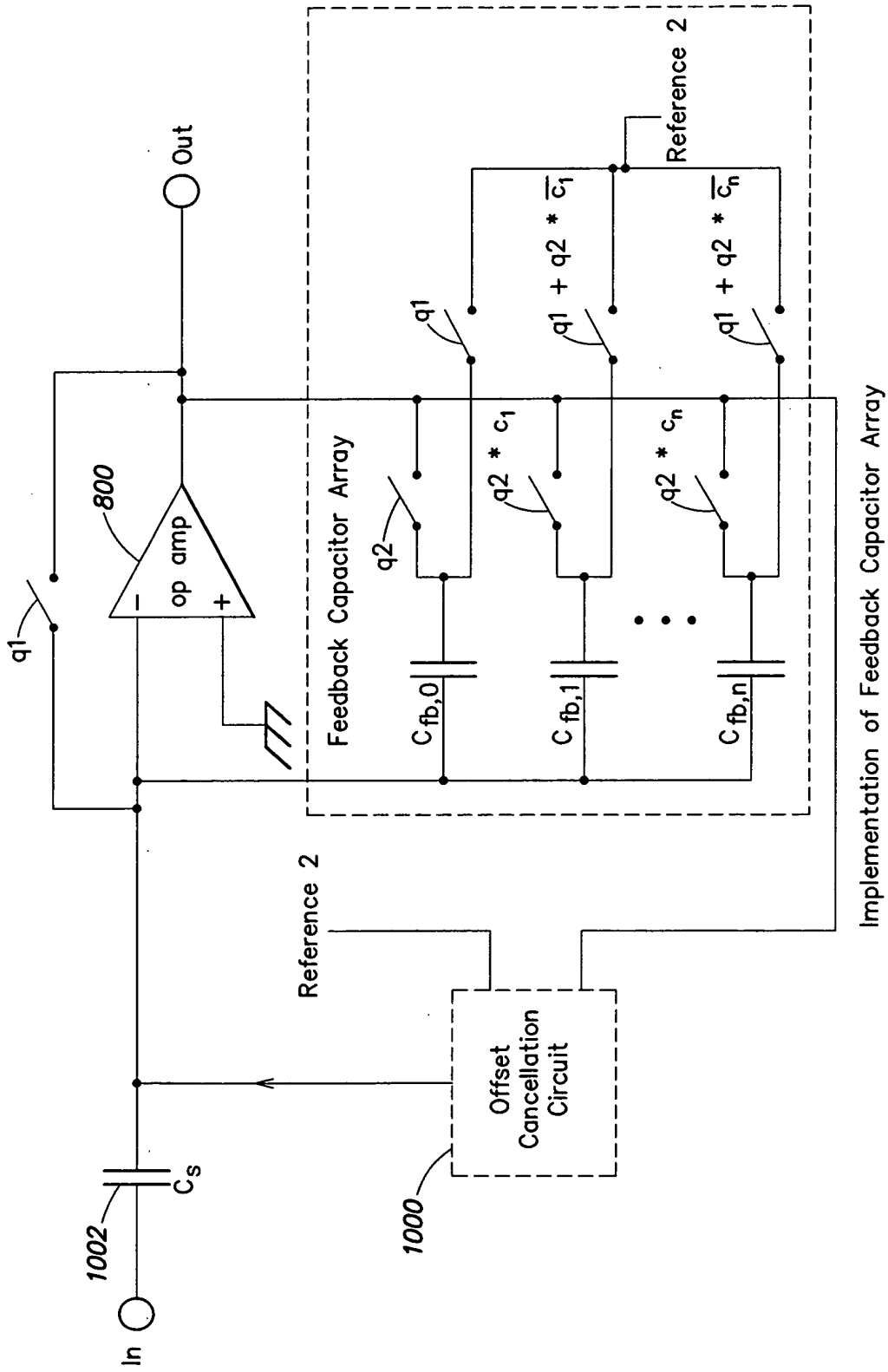
Out
In
800
op amp
q1
Feedback Capacitor Array
q2
q2 * c1
q2 * cn
Cfb,0
Cfb,1
Cfb,n
Reference 2
q1
q1 + q2 * c1
q1 + q2 * cn
Implementation of Feedback Capacitor Array
Reference 2
Offset Cancellation Circuit
1000
1002
Cs

FIG. 11